Notice of Allowability	Application No.	Applicant(s)	
	09/688,803	NAKAMURA, YOSHIYUKI	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/15/2004*.

2. ☒ The allowed claim(s) is/are *1-3,8 and 9*.

3. ☒ The drawings filed on *25 July 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *12/15/2004* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Guy J Lamarre
Primary Examiner

EXAMINER'S AMENDMENT

An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to Applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this Examiner's amendment was given in a telephone interview with David A. Blumenthal (310-795-7895) on Wednesday, December 15, 2004.

Please amend the application as follows:

Amend the Title to Read:

-- TEST CIRCUIT METHOD AND APPARATUS --

Amend the Abstract as follows:

ABSTRACT

A test circuit for integrated circuit devices ~~is disclosed, which can shorten~~ shortens ~~the~~ test times, and ~~can reduce~~ reduces the length of the test pattern and the number of external terminals. The test circuit is provided between first and second target circuits, and incorporates ~~comprises~~ a first selection section for selecting one of a first output signal from the first target circuit, a second output signal from the second target circuit, and a test signal indicating a test pattern input via a test pattern input terminal., ~~according to first and second test mode signals supplied from an external device; a section for~~ A temporarily data storage section stores ~~storing~~ the signal selected by the first section ~~as a data signal;~~, and a second selection selects ~~a section for selecting~~ one of ~~the~~ temporarily stored data ~~signal~~ or the second output signal. The results are provide ~~according to the second test mode signal, and providing the selected signal~~ to the first target circuit. A third selecting section is provided; ~~and a section~~ for selecting one of the temporarily stored data ~~signal~~ or the first output signal ~~according to a third test mode signal supplied from an external device,~~ and providing the selected signal to the second target circuit. ~~The temporarily stored data signal is also output as a test result via a test pattern output terminal.~~

Amend the Claims as follows:

In Claim 1:

A test circuit, provided between first and second target circuits, for testing the target circuits, comprising:

a first selecting section for selecting and outputting one of three input signals, namely: (1) a first output signal output from the first target circuit, (2) a second output signal output from the second target circuit, and (3) a test signal indicating a test pattern input via a test pattern input terminal, said selection being made according to first and second test mode signals supplied to said first selecting section as additional inputs used for selection, said first and second test mode signals supplied from an external device;

a temporary data storage section for temporarily storing the signal selected by the first selecting section as a data signal;

a second selecting section for selecting, as a first selection signal~~signal~~ one of either the temporarily stored data signal stored in said temporary data storage section or the second output signal from the second target circuit according to the second test mode signal fed to said second selecting section as a selection input, and providing the first selected signal to the first target circuit; and

a third selecting section for selecting, as a second selecting signal, one of the temporarily stored data signal or the first output signal from the first target circuit according to a third test mode signal supplied from said external device, and providing the second selected signal to the second target circuit, and wherein:

the temporarily stored data signal is also output as a test result via a test pattern output terminal.

Reasons for Allowance

Claims 1-3, 8 and 9 are allowed. The following is an Examiner's reasoned statement for allowance.

Independent claim 1 of the present application teaches a test circuit, provided between first and second target circuits, for testing the target circuits, comprising: a first selecting section for selecting and outputting one of three input signals, namely: (1) a first output signal output from the first target circuit, (2) a second output signal output from the second target circuit, and (3) a test signal indicating a test pattern input via a test pattern input terminal, said selection being made according to first and second test mode signals supplied to said first selecting section as additional inputs used for selection, said first and second test mode signals supplied from an external device; a temporary data storage section for temporarily storing the signal selected by the first selecting section as a data signal; a second selecting section for selecting, as a first data storage section or the second output signal from the second target circuit according to the second test mode signal fed to said second selecting section as a selection input, and providing the first selected signal to the first target circuit; and a third selecting section for selecting, as a second selecting signal, one of the temporarily stored data signal or the first output signal from the first target circuit according to a third test mode signal supplied from said external device, and providing the second selected signal to the second target circuit, and wherein: the temporarily stored data signal is also output as a test result via a test pattern output terminal. The forgoing limitations are taught by the prior arts of record. The prior art of record, namely James, teaches a method and apparatus for dynamically configuring the number of boundary-scan cells in a boundary-scan path is disclosed. A plurality of control signals is asserted to a plurality of

boundary-scan cells in a boundary-scan path. Each control signal of the plurality of control signals is in a first state or a second state. For each control signal that is in a first state, a respective one of the plurality of boundary-scan cells is bypassed in the boundary-scan path. None of the prior arts of record teach nor fairly suggest all the limitations in the independent claim 1 of the present application. In particular, the limitations of "...a first selecting section for selecting and outputting one of three input signals, namely: (1) a first output signal output from the first target circuit, (2) a second output signal output from the second target circuit, and (3) a test signal indicating a test pattern input via a test pattern input terminal, said selection being made according to first and second test mode signals supplied to said first selecting section as additional inputs used for selection, said first and second test mode signals supplied from an external device; a temporary data storage section for temporarily storing the signal selected by the first selecting section as a data signal; a second selecting section for selecting, as a first data storage section or the second output signal from the second target circuit according to the second test mode signal fed to said second selecting section as a selection input, and providing the first selected signal to the first target circuit; and a third selecting section for selecting, as a second selecting signal, one of the temporarily stored data signal or the first output signal from the first target circuit according to a third test mode signal supplied from said external device, and providing the second selected signal to the second target circuit, and wherein: the temporarily stored data signal is also output as a test result via a test pattern output terminal..." are not taught nor fairly suggested in the prior arts of record.

Independent claim 9 includes similar limitations as independent claim 1 and therefore is allowed for similar reasons.

Dependent claims 2, 3 and 8 depend from independent claim 1 and inherently include limitations therein and therefore are allowed as well.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
December 16, 2004

Gregory J Lamarre
Primary Examiner